FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11114-1E

MEMORY

Buffered

4 M × 72 BIT SYNCHRONOUS DYNAMIC RAM DIMM

MB8504S072AD-100/-84/-67

200-pin, 1-bank, based on 4 M × 4 BIT SDRAMs with PLL

■ DESCRIPTION

The Fujitsu MB8504S072AD is a fully decoded, CMOS Synchronous Dynamic Random Access Memory (SDRAM) module consisting of eighteen MB81117422A devices which organized as two banks of 1 M × 8 bits. This module is possible to minimize the skews of input signals such as clock and address signal by the PLL clock driver and register buffers mounted. The MB8504S072AD is optimized for those applications requiring high speed, high performance and large memory storage, and high density memory organizations.

This module is ideally suited for supercomputers, workstations, high-end PCs, laser printers, high resolution graphic adapters, accelerators, and other applications where a simple interface is needed.

■ PRODUCT LINE & FEATURES

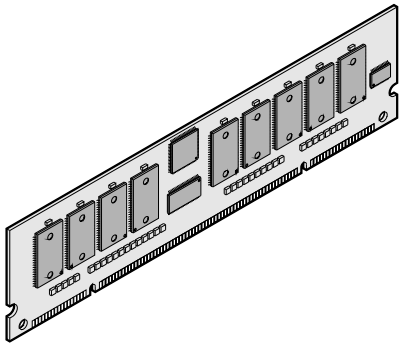
Parameter		MB8504S072AD-100	MB8504S072AD-84	MB8504S072AD-67
Clock Frequency		100 MHz max.	84 MHz max.	67 MHz max.
Burst Mode Cycle Time		10 ns max. (CL = 4) 15 ns max. (CL = 3)	12 ns max. (CL = 4) 17 ns max. (CL = 3)	15 ns max. (CL = 4) 20 ns max. (CL = 3)
$\overline{RAS}$ Access Time		54.5 ns max.	56.5 ns max.	60.5 ns max.
$\overline{CAS}$ Access Time		24.5 ns max.	26.5 ns max.	30.5 ns max.
Output Valid from Clock		9 ns max. (CL = 4) 9.5 ns max. (CL = 3)	9 ns max. (CL = 4) 9.5 ns max. (CL = 3)	9.5 ns max. (CL = 4) 10.5 ns max. (CL = 3)
Power Dissipation	Burst Mode	9968 mW max.	9122 mW max.	8276 mW max.
	Power Down Mode	572 mW max.	508 mW max.	443 mW max.

- Buffered 200-pin DIMM Socket Type
  (Lead pitch: 1.27 mm)
- Conformed to JEDEC Standard
- Organization: 4,194,304 words × 72 bits (ECC)
- Memory: MB81117422A (4 M × 4, 2-bank) × 18 pcs.
- 3.3 V ±0.3 V Supply Voltage
- All input/output LVTTL compatible
- 2048 Refresh Cycle every 32.8 ms (Burst Refresh)
- Auto and Self Refresh
- CKE Power Down Mode
- Output Enable and Input Data Mask
- PLL Clock Driver/Register Buffer/Input Buffer
- Module size:
  1.5” (height) × 6.05” (length) × 0.16” (thick)

MB8504S072AD-100/-84/-67

■ PACKAGE

Plastic DIMM Package



(MDS-200P-P07)

Package and Ordering Information

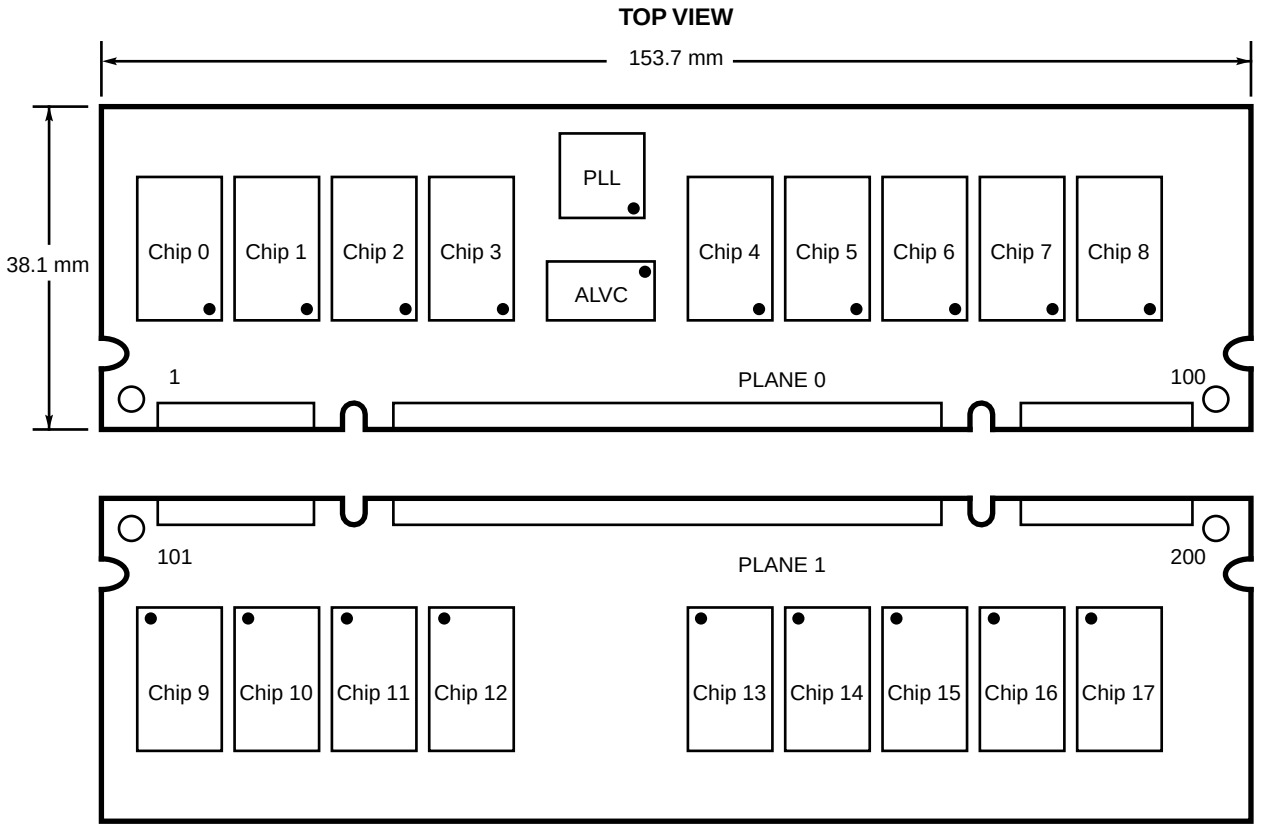
– 200-pad DIMM, order as MB8504S072AD-××DG (DG = Gold Pad)

MB8504S072AD-100/-84/-67

■ PIN ASSIGNMENTS

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V_{CC}	41	V_{SS}	81	DQ_{15}	121	DQ_{56}	161	V_{SS}
2	N.C.	42	A_8	82	DQ_{14}	122	V_{CC}	162	DQ_{31}
3	N.C.	43	A_9	83	V_{SS}	123	DQ_{55}	163	DQ_{30}
4	IN	44	V_{CC}	84	DQ_{13}	124	DQ_{54}	164	V_{CC}
5	OUT	45	N.C. (CKE_1)	85	DQ_{12}	125	V_{SS}	165	DQ_{29}
6	ID_0	46	CKE_0	86	V_{CC}	126	DQ_{53}	166	DQ_{28}
7	ID_1	47	V_{SS}	87	DQ_7	127	DQ_{52}	167	V_{SS}
8	V_{SS}	48	$\overline{CAS}$	88	DQ_6	128	V_{CC}	168	DQ_{23}
9	DQ_{67}	49	N.C.	89	V_{SS}	129	DQ_{47}	169	DQ_{22}
10	DQ_{66}	50	V_{CC}	90	DQ_5	130	DQ_{46}	170	V_{CC}
11	V_{CC}	51	V_{SS}	91	DQ_4	131	V_{SS}	171	DQ_{21}
12	DQ_{65}	52	$\overline{RAS}$	92	V_{CC}	132	DQ_{45}	172	DQ_{20}
13	DQ_{64}	53	V_{SS}	93	$\overline{PDE}$	133	DQ_{44}	173	V_{SS}
14	V_{SS}	54	N.C.	94	PD_1	134	V_{CC}	174	N.C.
15	DQ_{63}	55	N.C.	95	PD_2	135	DQ_{39}	175	N.C.
16	DQ_{62}	56	V_{CC}	96	PD_3	136	DQ_{38}	176	V_{CC}
17	N.C.	57	A_0	97	PD_4	137	V_{SS}	177	N.C.
18	DQ_{61}	58	A_1	98	N.C.	138	DQ_{37}	178	V_{SS}
19	DQ_{60}	59	V_{SS}	99	N.C.	139	DQ_{36}	179	V_{SS}
20	V_{CC}	60	DQ_{35}	100	V_{SS}	140	V_{CC}	180	N.C.
21	N.C.	61	DQ_{34}	101	N.C.	141	A_6	181	N.C.
22	N.C.	62	V_{CC}	102	N.C.	142	A_7	182	V_{CC}
23	V_{SS}	63	DQ_{33}	103	V_{SS}	143	V_{SS}	183	DQ_{11}
24	N.C.	64	DQ_{32}	104	N.C.	144	A_{11}	184	DQ_{10}
25	N.C.	65	V_{SS}	105	N.C.	145	N.C.	185	V_{SS}
26	V_{CC}	66	DQ_{27}	106	N.C.	146	V_{CC}	186	DQ_9
27	DQ_{51}	67	DQ_{26}	107	ID_2	147	DQM	187	DQ_8
28	DQ_{50}	68	V_{CC}	108	DQ_{71}	148	$\overline{WE}$	188	V_{CC}
29	V_{SS}	69	DQ_{25}	109	DQ_{70}	149	V_{SS}	189	DQ_3
30	DQ_{49}	70	DQ_{24}	110	V_{SS}	150	N.C.	190	DQ_2
31	DQ_{48}	71	V_{SS}	111	DQ_{69}	151	CLK	191	V_{SS}
32	V_{CC}	72	DQ_{19}	112	DQ_{68}	152	V_{CC}	192	DQ_1
33	DQ_{43}	73	DQ_{18}	113	V_{CC}	153	N.C. ($\overline{CS_1}$)	193	DQ_0
34	DQ_{42}	74	V_{CC}	114	N.C.	154	$\overline{CS_0}$	194	PD_5
35	V_{SS}	75	DQ_{17}	115	V_{SS}	155	V_{SS}	195	PD_6
36	DQ_{41}	76	DQ_{16}	116	N.C.	156	N.C.	196	PD_7
37	DQ_{40}	77	V_{SS}	117	DQ_{59}	157	A_{10}	197	PD_8
38	V_{CC}	78	N.C.	118	DQ_{58}	158	V_{CC}	198	V_{CC}
39	A_4	79	N.C.	119	V_{SS}	159	A_2	199	N.C.
40	A_5	80	V_{CC}	120	DQ_{57}	160	A_3	200	N.C.

MB8504S072AD-100/-84/-67



(MDS-200P-P07)

■ PIN DESCRIPTION

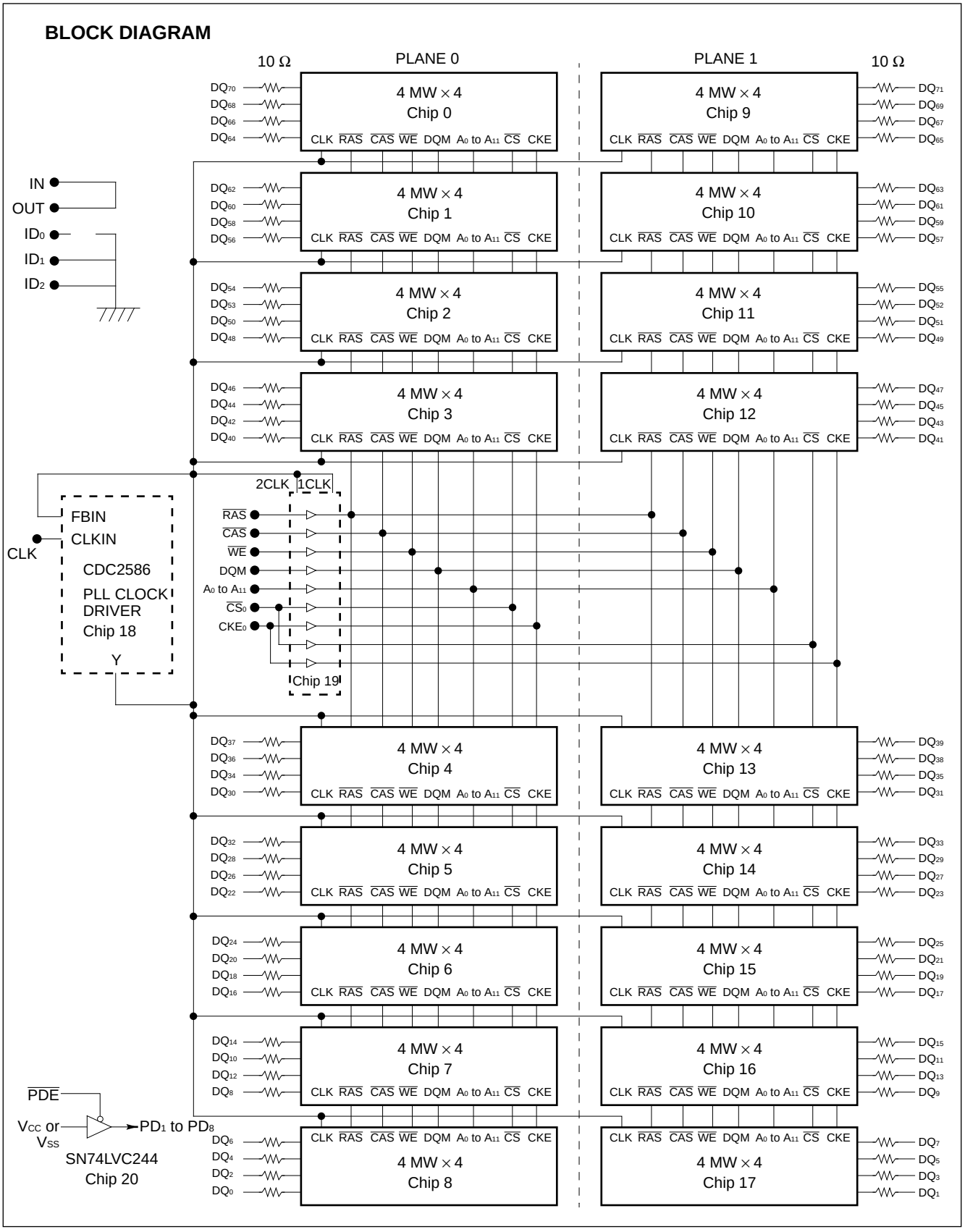
Symbol	I/O	Function	Symbol	I/O	Function
A_0 to A_{11}	I	Address Input	DQ_0 to DQ_{71}	I/O	Data Input/Data Output
$\overline{RAS}$	I	Row Address Strobe	V_{CC}	—	Power Supply (+3.3 V)
$\overline{CAS}$	I	Column Address Strobe	V_{SS}	—	Ground (0 V)
$\overline{WE}$	I	Write Enable	N.C.	—	No Connection
DQM	I	Data (DQ) Mask	PD_1 to PD_8	O	Presence Detect
CLK	I	Clock Input	ID_0 to ID_2	O	ID bit
CKE_0	I	Clock Enable	$\overline{PDE}$	I	Precence Detect Enable
$\overline{CS_0}$	I	Chip Select			

■ PRESENCE DETECT(PD)/ID DEFINITION

Symbol	MB8504S072AD -100	MB8504S072AD -84	MB8504S072AD -67	Description of PD/ID
PD_1	L	L	L	MODULE CONFIGURATION, SDRAM ORGANIZATION, AND ADDRESSING; Module Configuration: 4 M × 72 Mounted SDRAM Configuration: 4 M × 4 SDRAM Address (Row/Column): 12/10
PD_2	H	H	H	
PD_3	L	L	L	
PD_4	H	H	H	
PD_5	H	L	H	MODULE SPEED; 10 ns: PD_5 = H, PD_6 = L 12 ns: PD_5 = L, PD_6 = H 15 ns: PD_5 = H, PD_6 = H
PD_6	L	H	H	
PD_7	H	H	H	BUFFERING; Buffered: PD_7 = H
PD_8	H	H	H	BYTE WRITE; Word: PD_8 = H
ID_0	OPEN	OPEN	OPEN	COLUMN TO COLUMN COMMAND INTERVAL; 1 Clock: ID_0 = OPEN
ID_1	V_{SS}	V_{SS}	V_{SS}	READ PRECHARGE POSITION; No Early RAS: $ID_1 = V_{SS}$
ID_2	V_{SS}	V_{SS}	V_{SS}	POWER; Normal: $ID_2 = V_{SS}$

MB8504S072AD-100/-84/-67

BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value		Unit
		Min.	Max.	
Supply Voltage*	V_{CC}	–0.5	+4.6	V
Input Voltage*	V_{IN}	–0.5	+4.6	V
Output Voltage*	V_{OUT}	–0.5	+4.6	V
Storage Temperature	T_{STG}	–55	+125	°C
Power Dissipation	P_D	—	25	W
Output Current (D.C.)	I_{OUT}	–50	+50	mA

* : Voltages referenced to V_{SS} (= 0 V)

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Value			Unit
			Min.	Typ.	Max.	
Supply Voltage	*1	V_{CC}	3.0	3.3	3.6	V
		V_{SS}	0	0	0	V
Input High Voltage, All Inputs	*1	V_{IH}	2.0	—	V_{CC} +0.5	V
Input Low Voltage, All Inputs	*1	V_{IL}	–0.5	—	0.8	V
Ambient Temperature		T_A	0	—	+70	°C

*1. Voltages referenced to V_{SS} (= 0 V)

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ CAPACITANCE

(V_{CC} = +3.3 V, f = 1 MHz, T_A = +25°C)

Parameter		Symbol	Value		Unit
			Min.	Max.	
Input Capacitance	A_0 to A_{11}	C_{IN1}	—	10	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	10	pF
	$\overline{CS}$	C_{IN3}	—	14	pF
	CKE_0	C_{IN4}	—	14	pF
	CLK	C_{IN5}	—	10	pF
	DQM	C_{IN6}	—	10	pF
Input/Output Capacitance	DQ_0 to DQ_{71}	C_{DQ}	—	13	pF

MB8504S072AD-100/-84/-67

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes		Symbol	Condition	Value		Unit
					Min.	Max.	
Operating Current (Average Power Supply Current)	*2	MB8504S072AD-100	I_{CC1S}	No Burst; t_{CK} = min t_{RC} = min One Bank Active	—	1701	mA
		MB8504S072AD-84			—	1584	mA
		MB8504S072AD-67			—	1467	mA
		MB8504S072AD-100	I_{CC1D}	No Burst; t_{CK} = min t_{RC} = min All Banks Active	—	2576	mA
		MB8504S072AD-84			—	2358	mA
		MB8504S072AD-67			—	2140	mA
Precharge Standby Current (Power Supply Current)	*2	MB8504S072AD-100	I_{CC2P}	CKE = V_{IL}, t_{CK} = min All Banks Idle	—	159	mA
		MB8504S072AD-84			—	141	mA
		MB8504S072AD-67			—	123	mA
		MB8504S072AD-100	I_{CC2N}	CKE = V_{IH}, t_{CK} = min All Banks Idle	—	636	mA
		MB8504S072AD-84			—	621	mA
		MB8504S072AD-67			—	607	mA
Active Standby Current (Power Supply Current)	*2	MB8504S072AD-100	I_{CC3P}	CKE = V_{IL}, t_{CK} = min Any Bank Active	—	636	mA
		MB8504S072AD-84			—	621	mA
		MB8504S072AD-67			—	607	mA
		MB8504S072AD-100	I_{CC3N}	CKE = V_{IH}, t_{CK} = min Any Bank Active	—	996	mA
		MB8504S072AD-84			—	981	mA
		MB8504S072AD-67			—	967	mA
Burst Mode Current (Average Power Supply Current)	*2	MB8504S072AD-100	I_{CC4}	t_{CK} = min	—	2769	mA
		MB8504S072AD-84			—	2534	mA
		MB8504S072AD-67			—	2299	mA
Auto-refresh Current (Average Power Supply Current)	*2	MB8504S072AD-100	I_{CC5}	Auto Refresh t_{CK} = min t_{RC} = min t_{RRD} = min	—	2098	mA
		MB8504S072AD-84			—	1899	mA
		MB8504S072AD-67			—	1701	mA
Self-refresh Current (Average Power Supply Current)		MB8504S072AD-100	I_{CC6}	t_{CK} = V_{IL}	—	159	mA
		MB8504S072AD-84			—	141	mA
		MB8504S072AD-67			—	123	mA
Input Leakage Current (All inputs except DQ)			$I_{I\,(L)}$	V_{IN} = 0 V	–10	10	µA
				V_{IN} = V_{CC}	–10	10	
Input Hold Current (All inputs except CLK, $\overline{PDE}$, DQ)			$I_{I\,(Hold)}$	V_{IN} = 0.0 V	75	—	µA
				V_{IN} = 2 V	—	–75	
Output Leakage Current (All DQ)			$I_{O\,(L)}$	Output is disabled (Hi-Z) 0 V ≤ V_{OUT} ≤ V_{CC} 3.0 V ≤ V_{CC} ≤ 3.6 V	–10	10	µA
LVTTL Output High Voltage	*1		V_{OH}	I_{OH} = –2.0 mA	2.4	—	V
LVTTL Output Low Voltage	*1		V_{OL}	I_{OL} = +2.0 mA	—	0.4	V

Notes: *1. Voltages referenced to V_{SS} (= 0 V)

*2. I_{CC} depends on the output termination, load conditions, clock cycle rate and signal clock rate. The specified values are obtained with the output open and no termination register.

*3. An initial pause (DESL on NOP) of 200 µs is required after power-on followed by a minimum of eight Auto-refresh cycles.

■ AC CHARACTERISTICS

(1) BASE CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Notes	Symbol	MB8504S072AD -100		MB8504S072AD -84		MB8504S072AD -67		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
1	Clock Period	CL = 4	t_{CK}	10	20	12	20	15	20	ns
		CL = 3		15	20	17	20	20	20	ns
2	Clock High Time		t_{CH}	4	—	4.8	—	6	—	ns
3	Clock Low Time		t_{CL}	4	—	4.8	—	6	—	ns
4	$\overline{CS}$ Set Up Time		t_{SC}	3.4	—	3.4	—	3.4	—	ns
5	$\overline{CS}$ Hold Time		t_{HC}	1	—	1	—	1	—	ns
6	Input Set Up Time		t_{SI}	3.4	—	3.4	—	3.4	—	ns
7	Input Hold Time		t_{HI}	1	—	1	—	1	—	ns
8	Data Input Set Up Time		t_{SID}	3.5	—	3.5	—	3.5	—	ns
9	Data Input Hold Time		t_{HID}	1.5	—	1.5	—	1.5	—	ns
10	Output Valid from Clock (t_{CLK} = min)	*1, *2 CL = 4	t_{AC}	—	9	—	9	—	9.5	ns
		CL = 3		—	9.5	—	9.5	—	10.5	
11	Output in Low-Z		t_{OLZ}	2.5	—	2.5	—	2.5	—	ns
12	Output in High-Z	*3	t_{OHZ}	2.5	—	2.5	—	2.5	—	ns
13	Output Hold Time		t_{OH}	2.5	—	2.5	—	2.5	—	ns
14	Time between Refresh		t_{REF}	—	32.8	—	32.8	—	32.8	ms
15	Transition Time		t_T	0.5	2	0.5	2	0.5	2	ns
16	Power Down Exit Time		t_{PDE}	3.5	—	4.5	—	5.5	—	ns

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(2) BASE VALUES FOR CLOCK COUNT/LATENCY

No.	Parameter	Notes	Symbol	MB8504S072AD -100		MB8504S072AD -84		MB8504S072AD -67		Unit
				Min.	Max.	Min.	Max.	Min..	Max.	
1	$\overline{RAS}$ Cycle Time	*4	t_{RC}	90	—	100	—	110	—	ns
2	$\overline{RAS}$ Access Time	*5	t_{RAC}	—	54.5	—	56.5	—	60.5	ns
3	$\overline{CAS}$ Access Time	*6, *9	t_{CAC}	—	24.5	—	26.5	—	30.5	ns
4	$\overline{RAS}$ Precharge Time		t_{RP}	30	—	35	—	40	—	ns
5	$\overline{RAS}$ Active Time		t_{RAS}	60	100000	65	100000	70	100000	ns
6	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*7	t_{RCD}	30	—	30	—	30	—	ns
7	Write Recovery Time		t_{WR}	10	—	12	—	15	—	ns
8	Write Precharge Time		t_{RWL}	10	—	12	—	15	—	ns
9	$\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time		t_{RRD}	30	—	30	—	30	—	ns

(3) CLOCK COUNT FORMULA (*8)

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \text{ (Round off a whole number)}$$

(4) LATENCY (The latency values on these parameters are fixed regardless of clock period.)

No.	Parameter		Symbol	MB8504S072AD -100	MB8504S072AD -84	MB8504S072AD -67	Unit
1	CKE to Clock Disable		l_{CKE}	2	2	2	Cycle
2	DQM to Output in High-Z		l_{DQZ}	3	3	3	Cycle
3	DQM to Input Data Delay		l_{DQD}	1	1	1	Cycle
4	Last Output to Write Command Delay		l_{OWD}	1	1	1	Cycle
5	Write Command to Input Data Delay		l_{DWD}	1	1	1	Cycle
6	Precharge to Output in High-Z Delay	CL = 4	l_{ROH}	4	4	4	Cycle
		CL = 3		3	3	3	Cycle
7	Mode Register Access to Bank Active (min)		l_{MRD}	2	2	2	Cycle
8	$\overline{CAS}$ to $\overline{CAS}$ Delay (min)		l_{CCD}	1	1	1	Cycle
9	$\overline{CAS}$ Bank Delay (min)		l_{CBD}	1	1	1	Cycle

Notes: *1. Assumes t_{RCD} and t_{CAC} are satisfied.

*2. t_{AC} also specifies the access time at burst mode except for first access.

*3. Specified where output buffer is no longer driven.

*4. Actual clock count of t_{RC} (I_{RC}) will be sum of clock count of t_{RAS} (I_{RAS}) and t_{RP} (I_{RP}).

*5. t_{RAC} is a reference value. Maximum value is obtained from the sum of t_{RCD} (min) and t_{CAC} (max).

*6. Assumes t_{RAC} and t_{AC} are satisfied.

*7. Operation within the t_{RCD} (min) ensures that t_{RAC} can be met; if t_{RCD} is greater than the specified t_{RCD} (min), access time is determined by t_{CAC} and t_{AC}.

*8. All base values are measured from the clock edge at the command input to the clock edge for the next command input.
All clock counts are calculated by a simple formula:
clock count equals base value divided by clock period (round off to a whole number).

*9. The I_{CAC} ($\overline{CAS}$ latency: CL) is programmed by the mode register.

*10. An initial pause (DESL on NOP) of 200 µs is required after power-up followed by a minimum of eight Auto-refresh cycles.

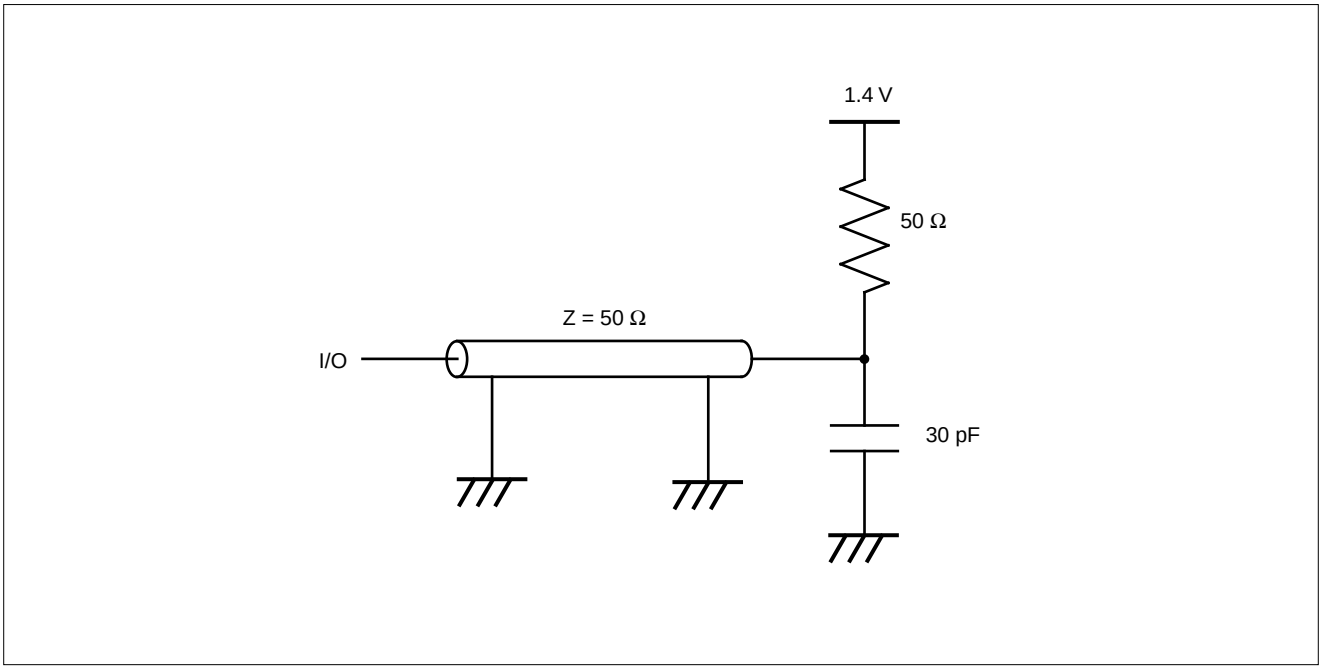
*11. 1.4 V or V_{REF} is the reference level for measuring timing of signals.
Transition times are measured between V_{IH} (min) and V_{IL} (max).

*12. AC characteristics assume t_T = 1 ns and 30 pF of capacitive load.

*Source: See MB81117422A Data Sheet for details on the electricals.

MB8504S072AD-100/-84/-67

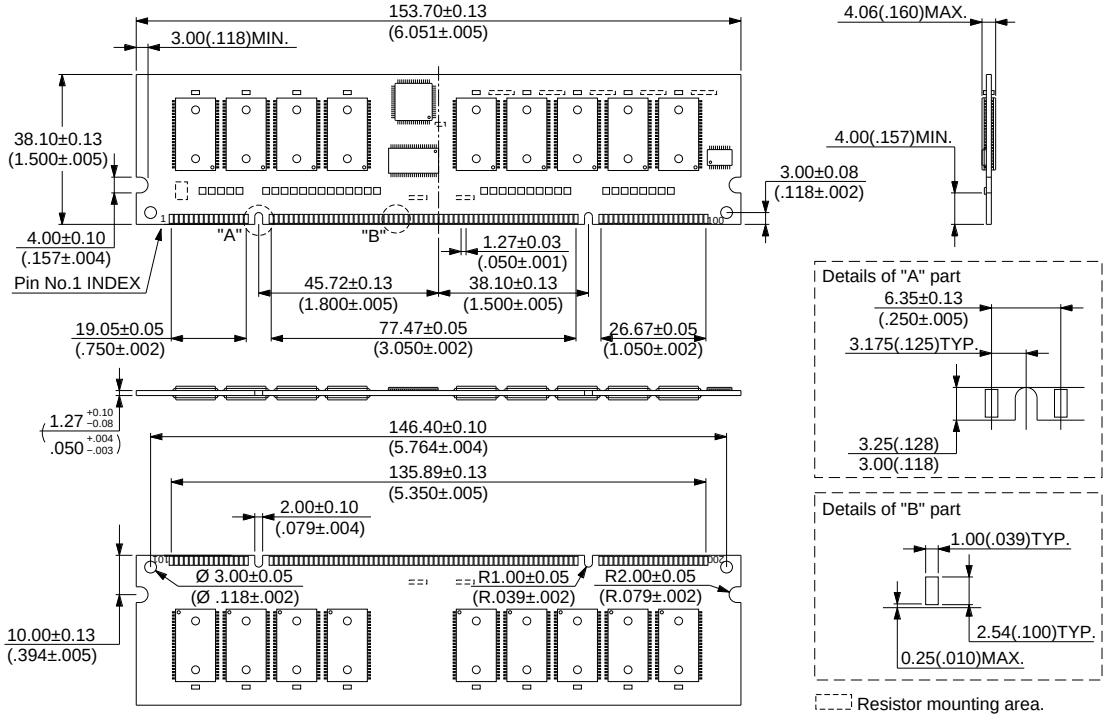
■ AC OPERATING TEST CONDITION (Example of AC Test Load Circuit)



MB8504S072AD-100/-84/-67

■ PACKAGE DIMENSION

200-PAD PLASTIC DUAL IN-LINE TYPE MODULE
(CASE No.: MDS-200P-P07)



Dimension in mm (inches)

MB8504S072AD-100/-84/-67

FUJITSU LIMITED

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CAUTION:
Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.